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IPMS TSN ETHERNET SUBSYSTEM | TSN_CRTL

Fraunhofer Institute for Photonic Microsystems IPMS

Maria-Reiche-Str. 2
01109 Dresden

Contact

Aron Guttowski
Phone +49 351 8823-229
aron.guttowski@ipms.fraunhofer.de

Dr. Frank Deicke
Phone +49 351 8823-385
frank.deicke@ipms.fraunhofer.de

www.ipms.fraunhofer.de

Overview

Time-Sensitive Networking (TSN) enhances Ethernet (specifically IEEE 802.1 and 802.3) and adds a variety of functions and capabilities. The goal is to make Ethernet more suitable for industrial applications requiring more deterministic characteristics than possible with present Ethernet standards. The IPMS TSN Ethernet Subsystem is an IP core to ease integration of devices into networks complying with TSN standards. It provides time-sensitive networking for full-duplex point-to-point Ethernet communication. The IP core consists of three sub-modules for time synchronization, traffic shaping and Ethernet MAC communication.

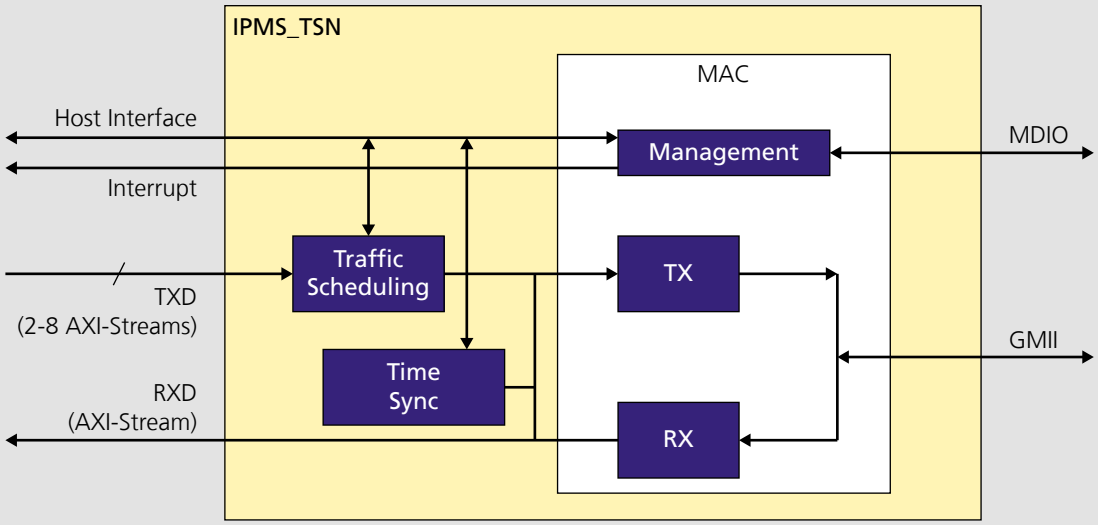
Applications

The TSN IP Core is suitable for the implementation of traffic sources and bridges for TSN Ethernet networks requiring robust, low-latency, and deterministic communication, mainly needed in industrial automation applications, such as robotics, automotive and conveyors.

Verification

Interoperability of sub-modules tested within TSN plug-fests by LNI4.0 and Industrial Internet Consortium (IIC).

industrial internet CONSORTIUM LNI4.0 LABS NETWORK INDUSTRIE 4.0



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Time Synchronization

- Supports IEEE 802.1as
- Clock synchronization to network grandmaster time
- Returns timestamps to the system using absolute time
- Includes periodic event triggers and alarms to assert host interrupt at specified absolute time
- Automatically calculates point-to-point latency
- Supports optional timer precision improvement by the host
- Supports time-aware end-points

Traffic Shaping

- Supports IEEE 802.1Qav and IEEE 802.1Qbv
- Supports 2 to 8 traffic classes, as per VLAN (IEEE 802.1Q)
- Enables bandwidth reservation and allocation per traffic class, and deterministic, low-latency, low-jitter communication for all traffic classes

Low Latency Ethernet MAC

- Supports IEEE 802.3
- Enables high-precision synchronization in TSN networks
- Triple speed: 10/100/1000 Mbit/s Ethernet
- PHY Interfaces to MII, GMII and RGMIII

Easy Integration

- APB4 Interface
- Other interfaces upon request

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Test benches
- Sample simulation and synthesis scripts
- Comprehensive documentation

Data Interfaces

- Advanced Peripheral Bus (APB) for memory mapped register access
- 2 - 8 AXI-Streams for TX data (configurable byte width)
- 1 AXI-Stream for RX data (configurable byte width)

1 *Schematic diagram of the TSN IP core.*