CAN-PCIe/402-FD

PCI Express® Board with 1 or 2 CAN-FD Interfaces

Single Lane PCIe Board with Altera® FPGA

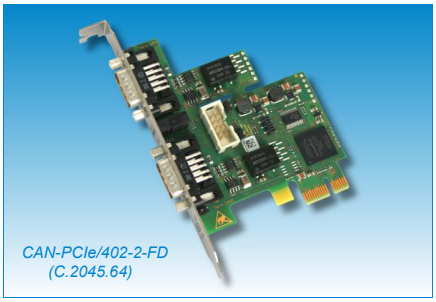
- 1x or 2x CAN-FD interfaces according to ISO 11898-2
- CAN bit rates from 10 kbit/s up to 5 Mbit/s with the same CAN transceiver
- Bus mastering and local data management by FPGA
- PCIe® interface according to PCI Express Specification R1.0a
- Selectable CAN termination on board
- Supports MSI (Message Signaled Interrupts)

Wide Range of Operating System Support and Advanced CAN Diagnostic

- Drivers and higher layer protocols for Windows®, Linux®, QNX®, RTX, RTX64 and others
- esd Advanced CAN Core (esdACC) technology

Variety of Product Designs

- Product versions available with or without electrical isolation
- Low profile version available



CAN-PCIe/402-2-FD (C.2045.64)

CAN-FD

The CAN-FD interface based on a modern FPGA based CAN core architecture (esdACC) is able to send and receive ISO conforming CAN-FD (up to 5 Mbit) or CAN 2.0 A/B messages. The CAN-FD bitrate range is validated from 10 kbit/s up to 5 Mbit/s.

Wide Choice of Hardware Designs

The CAN-PCIe/402-FD is a PC board designed for the PCIe bus that features one or two CAN-FD interfaces according to ISO 11898-2. These versions are also available without electrical isolation. Equipped with up to two CAN-FD interfaces the board is available as low profile versions (CAN-PCIe/402-1-LP-FD and -LP2-FD).

CAN Data Management

The independent CAN-FD nets according to ISO 11898-1:2015 are driven by the esdACC (esd Advanced CAN Core) implemented in the Altera FPGA. The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU load.

Due to the usage of MSI (Message Signaled Interrupts) the CAN-PCIe/402-FD can be operated for example in Hypervisor environments.
The CAN-PCIe/402-FD provides high resolution hardware timestamps.

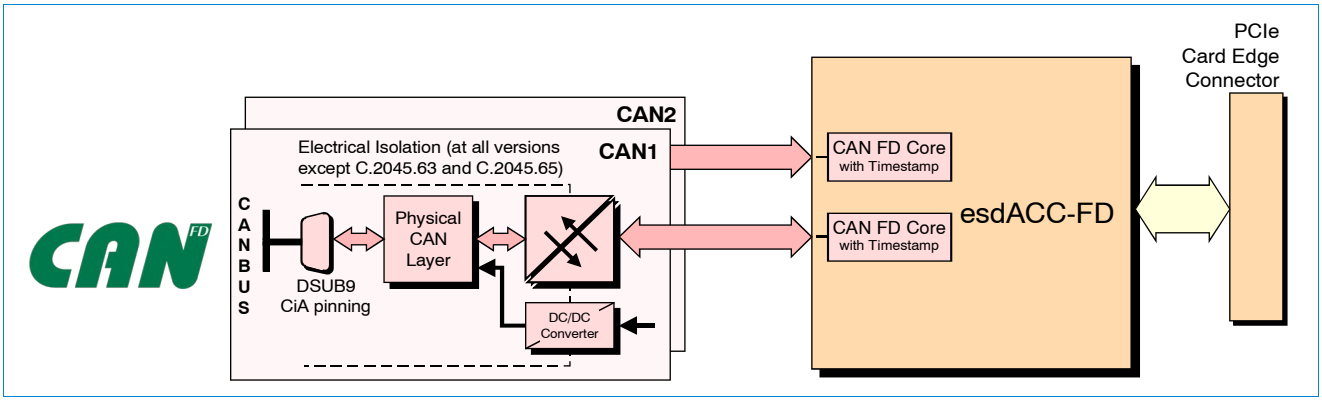
Software Support[1]

Windows and Linux (NTCAN-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Realtime OS (NTCAN-API)
CAN layer 2 drivers for QNX, RTX and RTX64 are available.

Higher Layer Protocols (non CAN FD)
Higher Layer Protocols are available for many operation systems (see order info):

- CANopen Master- and Slave-Stack
- J1939
- ARINC825



Technical Specifications:

PCI Express Interface:	
PCIe port	PCI Express Spec. R1.0a, Link width 1x

CAN:	
Interface	1x or 2x CAN-FD high-speed interfaces according to ISO 11898-2, bit rates from 10 kbit/s up to 5 Mbit/s (with the same CAN transceiver), with or without electrical isolation
CAN controller	esdACC in EP4CGX Altera FPGA, acc. to ISO 11898-1:2015

General:	
Ambient temp.	0 °C ... +75 °C
Rel. humidity	Max. 90 % (non-condensing)
Power suppy	3.3 V: 2x CAN I_{MAX} = 280 mA 12 V: 2x CAN I_{MAX} = 180 mA
Connector	PCIe: PCIe card edge connector CAN: 1x 9-pin DSUB per CAN channel, male
Weight	CAN-PCIe/402-2-FD: 60 g

Order Information:

Hardware		Order No.
CAN-PCIe/402-1-FD	1x CAN-FD (CAN 1 only)	C.2045.62
CAN-PCIe/402-1-D-FD	as C.2045.02 but without electr. isolation	C.2045.63
CAN-PCIe/402-2-FD	2x CAN-FD (CAN 1, CAN2)	C.2045.64
CAN-PCIe/402-2-D-FD	as C.2045.04 but without electr. isolation	C.2045.65
CAN-PCIe/402-1-LP-FD	Low profile version, 1x CAN-FD (CAN 1)	C.2045.92
CAN-PCIe/402-1-LP-2-FD	Low profile version, 1x CAN-FD (CAN 2)	C.2045.94

CAN layer 2 drivers for Windows and Linux are included in delivery.

Software Support[1]	
Additional CAN layer 2 object licenses including CD-ROM:	
CAN-DRV-LCD QNX	C.1101.32
CAN-DRV-LCD RTX (incl. RTX64)	C.1101.35
Higher CAN layer protocols including CD-ROM (for non CAN FD application only):	
CANopen-LCD Windows/Linux, RTX or QNX	C.1101.xx
J1939 stack for Windows and Linux	C.1130.xx
ARINC 825-LCD for Windows/Linux, RTX or QNX	C.1140.xx

[1] For detailed information about driver availability for your operating system please contact our sales team.

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CAN-PCIe/402-FD

Driven by esdACC-FD (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1:2015 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Bit rates from 10 kbit/s up to 5 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)
- Busload measurement

Superior esdACC Features [1]:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64 bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1:2015 conform
  - Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.

[1] Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.

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